WHAT IS CLAIMED IS:

1. A semiconductor testing apparatus comprising:

a read circuit for reading measurement data including a plurality of test vectors;

a measurement circuit for supplying the test vectors to semiconductor devices and for measuring a current value output from the semiconductor devices corresponding to each address of each test vector;

a calculation circuit for calculating a current-value change rate per address pair consisting of different two addresses;

a determination circuit for determining a range of pass/fail decision criteria to be used for deciding whether a semiconductor device as a target test device to be tested is a good sample or a fault sample based on current-value change rates obtained by supplying the plurality of test vectors to good samples as semiconductor devices; and

a decision circuit for comparing current-value change rates obtained by supplying the plurality of test vectors to faulty samples with the range of pass/fail decision criteria per address pair, and for deciding whether the target test device is a good sample as a non-defective semiconductor device or a faulty sample based on the current-value change rates corresponding to the address pairs extracted based on the comparison results obtained.

2. A semiconductor testing device according to claim 1, wherein the determination circuit determines the range of pass/fail decision criteria based on the current-value change rates obtained from the plurality of good samples.

3. A semiconductor testing device according to claim 1, wherein

the determination circuit comprising a measurement range

determination circuit for comparing current-value change rat s of the faulty samples obtained by supplying th plurality of test vectors to the faulty samples with the range of pass/fail decision criteria per address pair, and for extracting the address pairs corresponding to the current-value change rates of the faulty samples that are out of the range of pass/fail decision criteria from the plurality of address pairs in the plurality of test vectors, and for determining effective address pairs as an address pair group to be effectively used for the pass/fail decision,

wherein

the measurement circuit supplies the test vectors corresponding to the address pair group to the target test device.

4. A semiconductor testing device according to claim 3, wherein

the measurement range determination circuit compares the plural current-value change rates obtained from the plural faulty samples with the range of pass/fail decision criteria per address pair, and selects an effective address pair group, to be effectively more used for the pass/fail decision and according to the number of the plural faulty samples, from the address pair group of the plural test vectors in the address pairs corresponding to the current-value change rates of the plural faulty samples which are out of the range of pass/fail decision criteria.

5. A semiconductor testing method, comprising the steps of:

inputting a plurality of test vectors to semiconductor devices each being a good devices as a non-defective device, and measuring a current value output from each good sample corresponding to an address of each test v ctor, and outputting the measured current values as the current values of the good samples;

calculating a current-value change rate per address pair

forming two different addresses, and outputting this current-value change rate as the current-value change rate of the good sample;

determining a range of pass/fail decision criteria to be used for deciding whether a target test device to be tested is a good sample (non-defective sample) or a fault sample per address pair based on the above current-value change rates; and

supplying the plural test vectors to semiconductor devices as faulty samples, and measuring current values output from the above semiconductor devices as the faulty samples corresponding to the addresses, and outputting the measured current values as the current values of the faulty samples; and

comparing the current-value change rates of the measured current values corresponding to each address pair per address pair, and deciding whether a semiconductor device as a target test device to be tested is a good (non-defective) device or a faulty (defective) device based on the current-value change rates of the address pairs extracted based on the above comparison result.

6. A semiconductor testing method according to claim 5, wherein

the number of the semiconductor devices as the good samples is a plural number, and the current value and the current-value change rate of the good samples are output for each good sample, and the range of pass/fail decision criteria is determined based on the current-value change rates of the plural good samples.

7. A semiconductor testing method according to claim 5, further comprises the steps of:

supplying the plurality of test vectors to semiconductor devices as faulty samples, and measuring current values output from these semiconductor devices corresponding to the address pairs, and outputting the current values of the faulty samples;

calculating a change rate between the two current values

in the above current values corresponding to each address pair, and outputting the calculated results as current-value change rates of the faulty samples; and

comparing the current-value change rates of the faulty samples with the range of pass/fail decision criteria per address pair, and extracting effective address pairs, to be effectively used for the pass/fail decision, from the plural address pairs corresponding to the current-value change rates that are out of the range of pass/fail decision criteria,

wherein the step of measuring current values of the target test device is the step of measuring the current values by supplying the test vectors corresponding to the extracted effective address pairs for the pas/fail decision to the semiconductor device as the target test device.

8. A semiconductor testing method according to claim 7, wherein

the number of the semiconductor devices as the faulty samples are a plural number, and the current values and the current-value change rates of the faulty samples are output per faulty sample, the semiconductor testing method further comprises the steps of comparing the current-value change rates obtained from the plural faulty samples with the range of pass/fail decision criteria per address pair; and

extracting the address pair group as an effective combination to be effectively used for the pass/fail decision from the plural address pairs corresponding to the current-value change rates of the faulty samples that are out of the pass/fail decision criteria, according to the number of the faulty samples, and wherein

the step of measuring the current values of the target test device is the step of supplying the test vectors corresponding to the effective address pairs to be effectively used for the pass/fail decision to the semiconductor device as the target test device.

9. A program with which a semiconductor testing method is executed by a computer in a semiconductor testing apparatus which comprises: a read circuit for reading measurement data including test vectors; a measurement circuit for supplying the test vectors to a semiconductor device and for measuring current values output from the semiconductor device; and a decision circuit for deciding whether a semiconductor device as a target test device is a good device (non-defective device) or it is a defective device based on the current values,

the program comprising the procedures of:

inputting a plurality of test vectors to semiconductor devices as good (non-defective) samples, and measuring a current value corresponding to an address of each test vector output from the good sample, and outputting the measured current values as the current values of the good samples;

calculating a current-value change rate between two current values corresponding to an address pair forming two different addresses, and outputting the calculated current-value change rates as the current-value change rates of the good samples;

determining a range of pass/fail decision criteria to be used for the criteria of the pass/fail decision whether a target test device to be tested is a good sample or a fault sample per address pair based on the current-value change rates of the good samples;

supplying the plurality of the test vectors to semiconductor device as faulty samples, and measuring current values output from the semiconductor devices as the faulty samples corresponding to the addresses, and outputting the measured current values as the current values of the faulty sampl s;

calculating a current-value change rat of the two current values corresponding to each address pair, and outputting current-value change rates as the current-value change rates

of the faulty samples; and

comparing the curr nt-value change rate of the faulty samples with the range of pass/fail decision criteria per address pair, and deciding whether the semiconductor devices as the target test device is a good sample or a faulty sample based on the above comparison results.

10. A program with which a semiconductor testing method is executed by a computer in a semiconductor testing apparatus according to claim 9, wherein

the number of the semiconductor devices as the good samples is a plural number,

the current values and the current-value change rates of the good samples are output per good sample, and

the range of pass/fail decision criteria is determined based on the current-value change rates of the good samples.

11. A program with which a semiconductor testing method is executed by a computer in a semiconductor testing apparatus according to claim 9, further comprises the procedures of:

supplying the plurality of the test vectors to semiconductor devices as faulty samples, and measuring current values output from the above semiconductor devices corresponding to the addresses of the test vectors, and outputting the measured current values as the current values of the faulty samples; and

calculating a current-value change rate of the two current values corresponding to each address pair, and outputting the calculated results as the current-value change rates of the faulty samples; and

comparing the current-value change rates of the faulty samples with the range of pass/fail decision criteria per address pair, and extracting effective address pairs, to be effectively used for the pass/fail decision, from the plural address pairs corresponding to the curr nt-value change rates that are out of the range of pass/fail decision criteria,

wherein th step of measuring the current valu s of the target test device is the step of supplying th t st vectors corresponding to the above extracted effective test vectors to the semiconductor device as the target test device.

12. A program with which a semiconductor testing method is executed by a computer in a semiconductor testing apparatus according to claim 11, wherein

the number of the semiconductor devices as the faulty samples is a plural number, and the current values and the current-value change rates of the faulty samples are output per faulty sample;

the above program for executing the semiconductor testing method further comprises the following procedures:

the procedure of comparing the current-value change rates obtained from the plural faulty samples with the range of pass/fail decision criteria per address pair; and

the procedure of extracting the address pairs to be effectively used for the pass/fail decision from the plural address pairs corresponding to the current-value change rates of the faulty samples that are out of the pass/fail decision criteria, according to the number of the faulty samples,

and wherein

the procedure of measuring the current values of the target test device is the procedure of supplying the test vectors corresponding to the extracted effective address pairs to the semiconductor device as the target test device.

13. A semiconductor testing method of specifying a faulty part in a semiconductor product, comprising the steps of:

supplying a plurality of test vectors to good and faulty sampl s as semiconductor devices, and measuring current values corresponding to addresses indicating th test vectors;

calculating current-valu change rates between current values corresponding to an address pair consisting of two

addresses in each of th good and faulty samples; and

comparing th current-value change rates corr sponding to the address pairs in each of the good and faulty samples, and determining address pairs of the test vectors to be used for performing an emission analysis that is useful to specify a faulty part in a semiconductor device.

14. A semiconductor testing method of specifying a faulty part in a semiconductor product according to claim 13, further comprises the steps of:

performing an emission analysis for each of the good and faulty samples by using the test vectors obtained in the steps of determining the address pairs of the test vectors to be used for performing the emission analysis; and

specifying a faulty part by comparing emission patterns from the good sample with emission patterns from the faulty sampl e that have been obtained in the above emission analysis step.

15. A semiconductor testing method of specifying a faulty part in a semiconductor product according to claim 14, wherein

in the emission analysis step, different test vectors are supplied to each of the good and faulty samples in order to obtain emission patterns by changing the current values output from these samples, and

in the faulty part specifying step, the faulty part is specified by obtaining a difference of the change of the emission patterns in each of the good and faulty samples.

16. A semiconductor testing method of specifying a faulty part in a semiconductor product according to claim 15, further comprises the step of comparing the change of the emission parts in the good and faulty samples,

wherein in the faulty part sp cifying step, the emission area and the change of the emission area that do not occur in the good sample are detected and thereby the emission that is

unique to the faulty sample is decided as the faulty part relating to the defect.

17. A semiconductor testing method of specifying a faulty part in a semiconductor product according to claim 13, wherein

in the step of calculating the current-value change rate, two test vectors designated by two addresses are combined as an address pair, the range of the current-value change rates in the good and faulty samples are obtained according to the current-value change rates calculated by comparing the current values in optional number of the address pairs or in the test vectors in all the address pairs in each of the good and faulty samples.

18. A semiconductor testing method of specifying a faulty part in a semiconductor product according to claim 17, wherein

the current-value change rate between the test vectors per address pair in the faulty sample is compared with the current-value change rate between the test vectors in each address pair in the good sample, and

the test vector pairs in the condition that the current-value change rate obtained from the faulty sample is out of the range of the current-value change rate obtained from the faulty sample are searched, and these test vector pairs are decided as the test vector group to be used for the emission measurement, and the test vector group is extracted as the address pairs of the test vectors to be used for specifying a faulty part in a semiconductor device.

19. A semiconductor testing apparatus for specifying a faulty part in a semiconductor device, comprising:

a current-value change measuring circuit for supplying a plurality of test vectors to good and faulty samples as semiconductor devices, and for measuring a current value corresponding to each test vector;

a current-value change rate calculation circuit for calculating a current-value change rate per test vector pair in each of the good and faulty samples, the number of the test vector pairs being a desired number, by using the current values from the current-value measuring circuit;

an emission measurement address pair determination circuit for comparing the current-value change rates in each test vector pair in each of the good and faulty samples obtained by the current-value change rate calculation circuit, and for determining test vectors to be used in an emission analysis based on the comparison results;

an emission analysis circuit for performing the emission analysis using the test vectors determined above in each of the good and faulty samples; and

a faulty part determination circuit for comparing emission patterns of the good and faulty samples, and for specifying a faulty part in a semiconductor device based on the result of the emission pattern comparison.